

Altera Quartus II Tutorial

(For ECE 465 Students at UIC)

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Quartus II by Altera is a PLD Design Software which is suitable for high-density Field-Programmable Gate Array (FPGA) designs, low-cost FPGA designs, and Complex Programmable Logic Devices CPLD designs. The following tutorial is aimed to help UIC students taking ECE 465 course in designing their class projects.

The tutorial is organized as follows. First section gives pointers to Altera's website from where this software can be downloaded and instructions to install this software and obtaining license can be found. Second section describes a step by step approach to designing a simple 2 to 4 decoder using Quartus II's Schematic Editor. Finally the third section describes the simulation process of verifying the design of the decoder. Each section is augmented with figures of each step leading to the next process.

1. Downloading and Installing Quartus II

1.1 Download

The software can be downloaded from Altera's website (www.altera.com) at following URL.

https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp

1.2 Installation Instruction

Instructions to install the software can be found at the following URL.

https://www.altera.com/support/software/download/altera_design/quartus_we/ins-webdnl_consol.html

1.3 Setting up Licensing

Instructions to obtain the free academic personal license can be found at the following URL.

<https://www.altera.com/support/software/download/ins-license.html>

2 Creating Design Projects with Quartus II

In this section, we will learn to create a new project using Quartus II. For ease in understanding, I will go through each and every step in designing a simple digital circuit, a 2 to 4 decoder, with accompanying figures illustrating the step. The steps in creating a new project are as follows.

After we have successfully installed Quartus II and set up the license, we load the software, go to the file menu and select 'New Project Wizard'. This will open 'New Project Wizard' dialog box. The first screen asks us to provide names of the working directory of the project, name of the project and name of the top level entity in the project. We will have to fill all these fields with the relevant information. Figure1 illustrates this process.

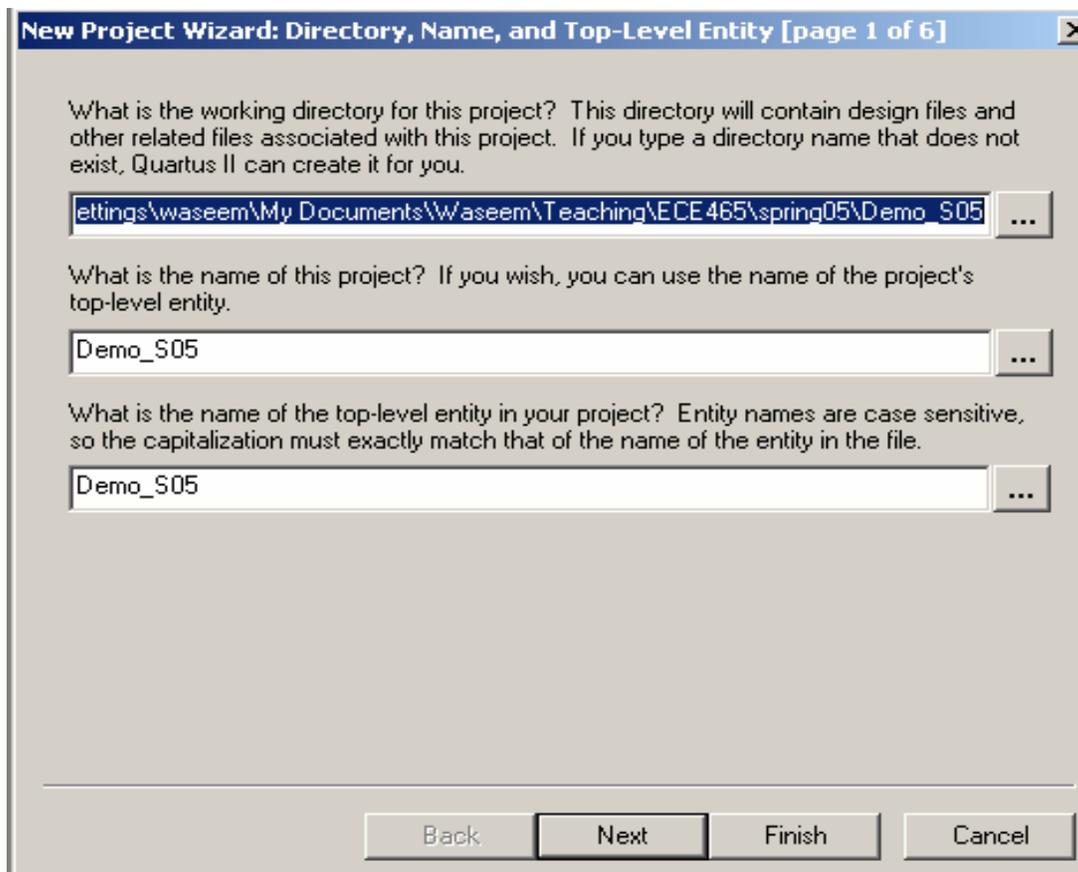


Figure1. First screen of the 'New Project Wizard' dialog box

The second screen asks us to add files to the project that we may have designed in advance. Since we don't have any such file to add, we will simply click next button to skip this step. The screen 2 is shown in figure2.

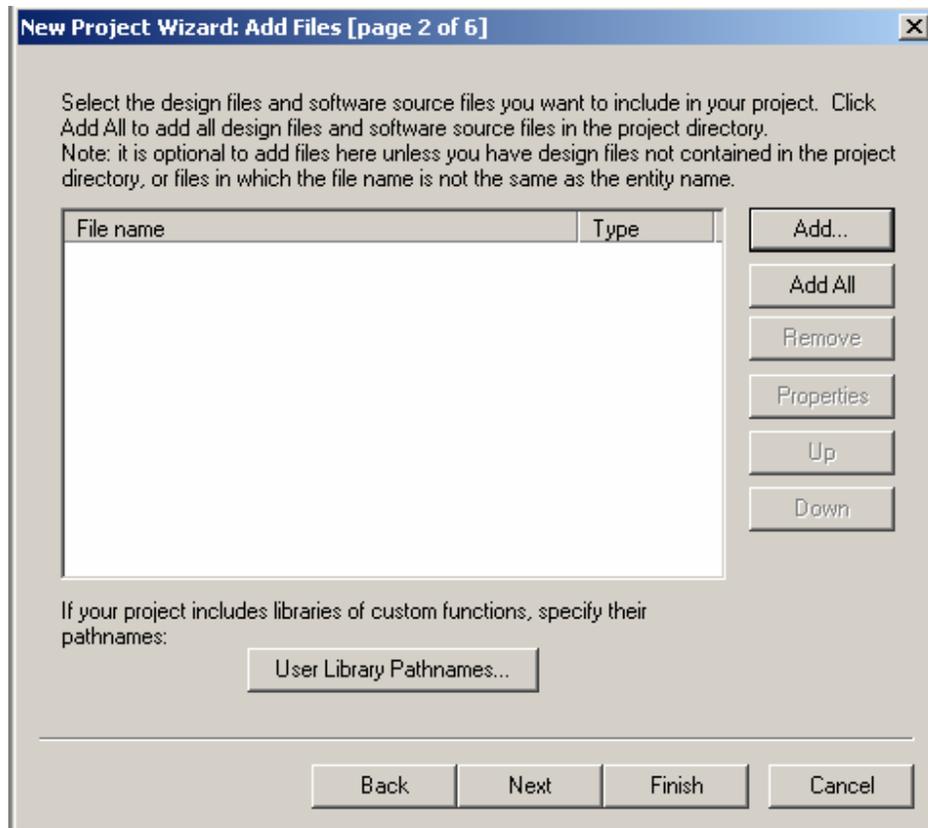


Figure2. Screen2 of the 'New Project Wizard' Dialog box

Quartus allows users familiar with other PLD tools to integrate their designs in those tools with Quartus II generated projects. Screen3 basically asks if there are other tools apart from Quartus II that we plan to use during the project. Since there are no such tools in our case, we will simply skip this process ob clicking 'next'. Screen3 is shown in figure 3.

Screen4 of the wizard asks us the target device family for our project. For all projects in ECE 465, we will let the compiler select the appropriate device. This step is shown in Figure4.

Screen 5 of the 'New Project Wizard' asks us to specify a list of devices so that the compiler can select one of them as the target device. For our case, default list will suffice. Screen5 is shown in Figure5.

Finally Screen6 tells us that the 'New Project Wizard' is finished and the new project with the shown settings is created. This step is shown in Figure6.

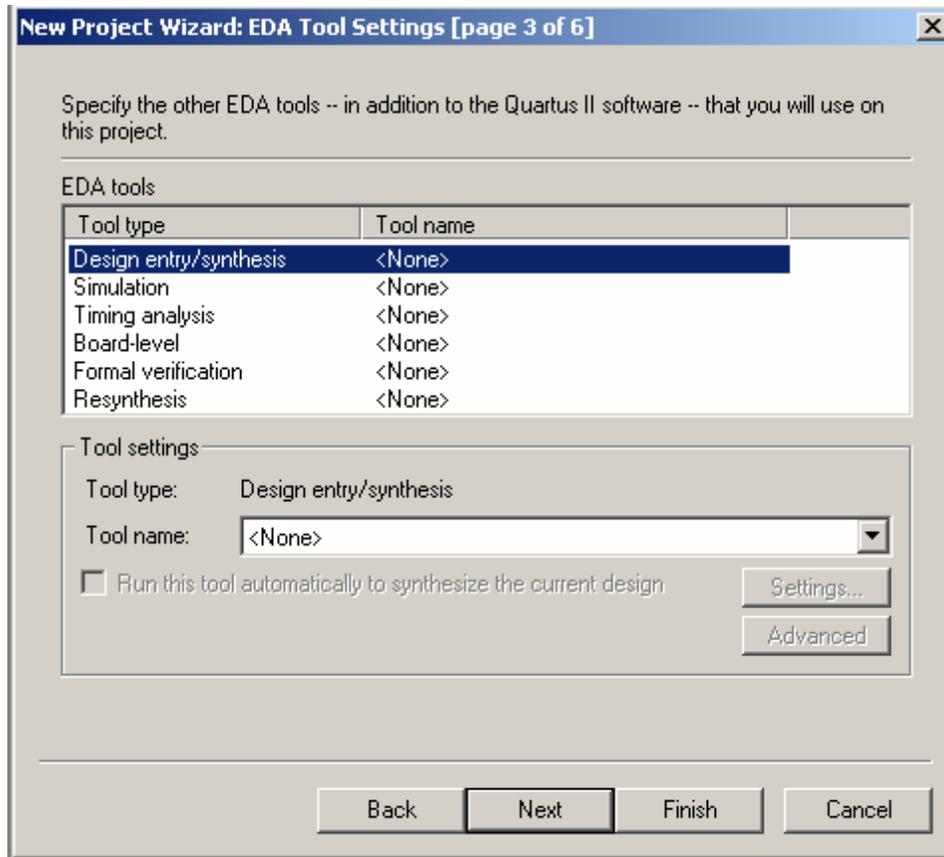


Figure3. Screen3 of the 'New Project Wizard'

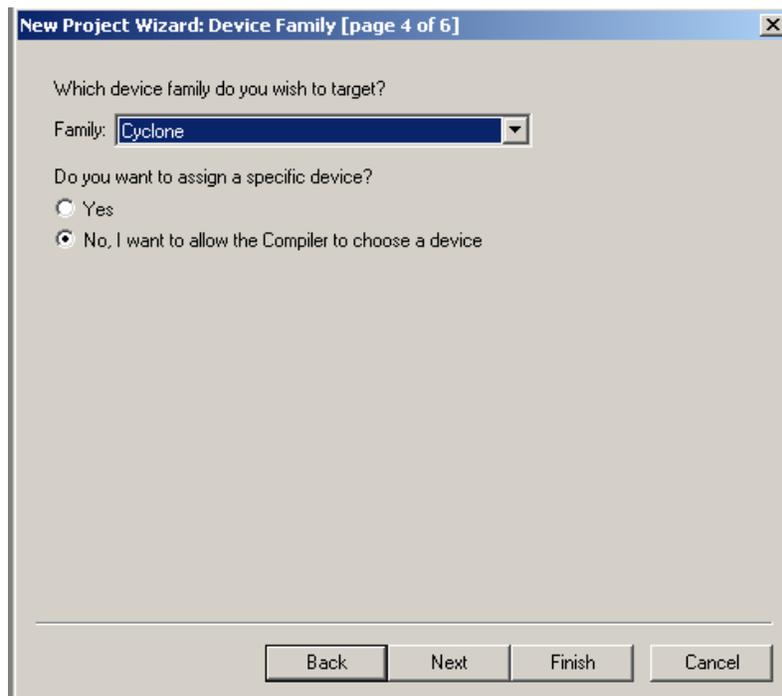


Figure4. Screen4 of the 'New Project Wizard'

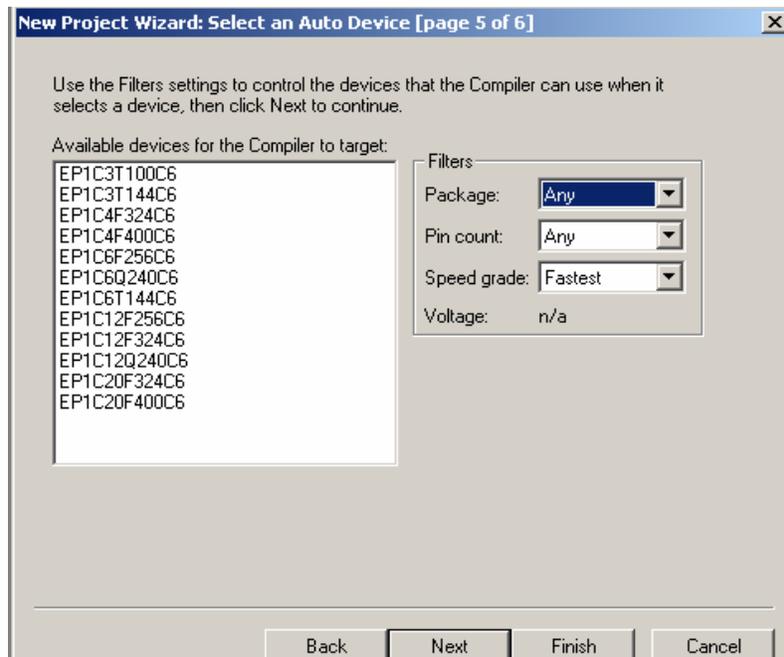


Figure5. Screen5 of the 'New Project Wizard'

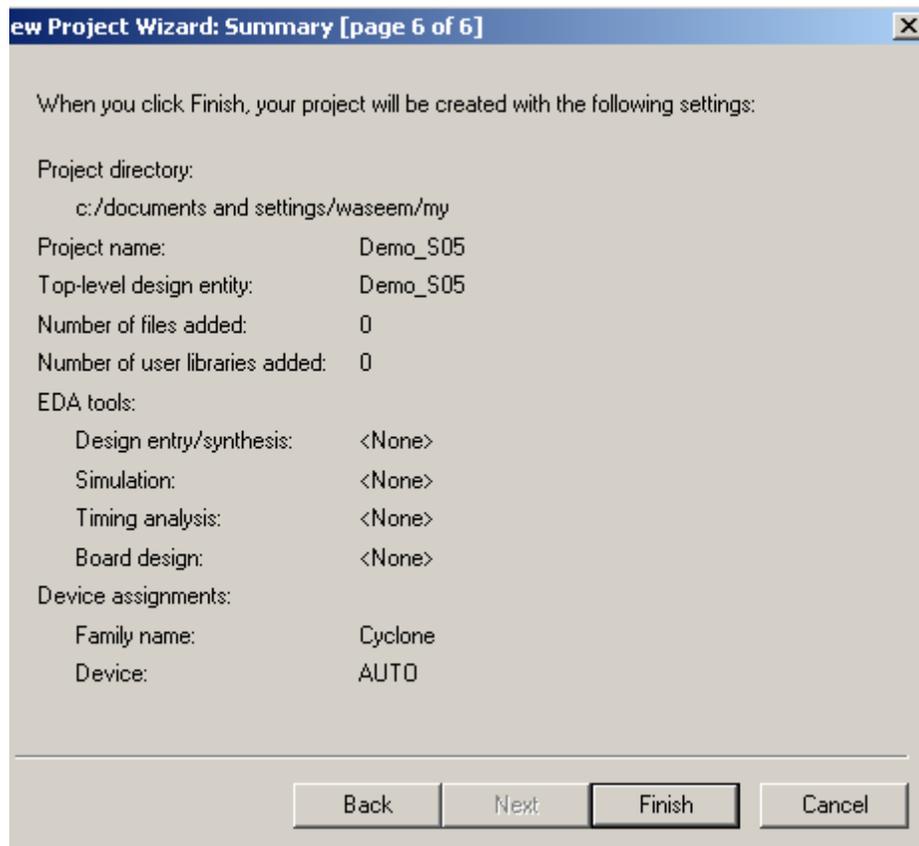


Figure6. Screen6 of the 'New Project Wizard'

Once we are done creating the project space, we now need to create design files for the project. We will use Block Diagram/Schematic File based design method throughout the course. To create a new design file, we go to file menu and select 'New' which will open the 'New File' Dialog box as shown in Figure7.

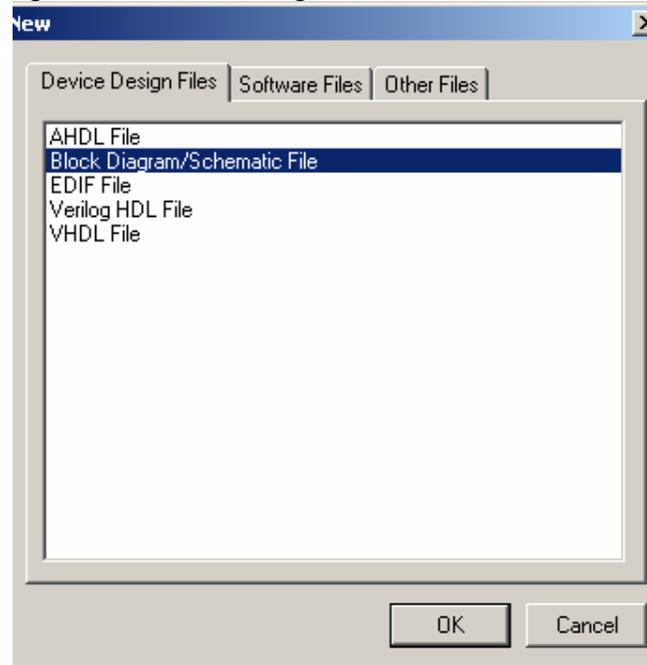


Figure7. Creating a new schematic based design file

Once we highlight the Block Diagram/Schematic File and press OK. Quartus II will open a schematic editor with an array of tools arranged in sidebar. Figure8 shows the toolbar holding schematic editor related tools. 'Symbol Tool' which we will use most frequently is highlighted. This tool has the shape of an AND gate.

In our example of decoder design, we will use this 'Symbol Tool' to place all the logic elements required for our decoder circuit i.e. four 'AND' gates and two 'NOT' gates as well as input and output pins. The procedure to place any element in the schematic file is very simple, we simply select that element using 'Symbol Tool' and place it on the schematic file by the click of mouse and keep on clicking till we have placed it for the required number of times. When we are done, we just press 'ESC' key and the mouse pointer returns to the normal arrow pointer. Figures 9-13 illustrate this process.

Figure14 shows all the logic elements, without wiring, placed in the schematic file design layout area. Figure15 shows how all these elements are connected to form the eventual decoder circuit.

Figure15 shows the step of saving the schematic design file. We must make sure that 'Add file to the Current Project' checkbox is in checked state while saving the file. After saving the file, we compile our project and if the compilation is successful, move to the next step of simulating the circuit which is explained in the next section.

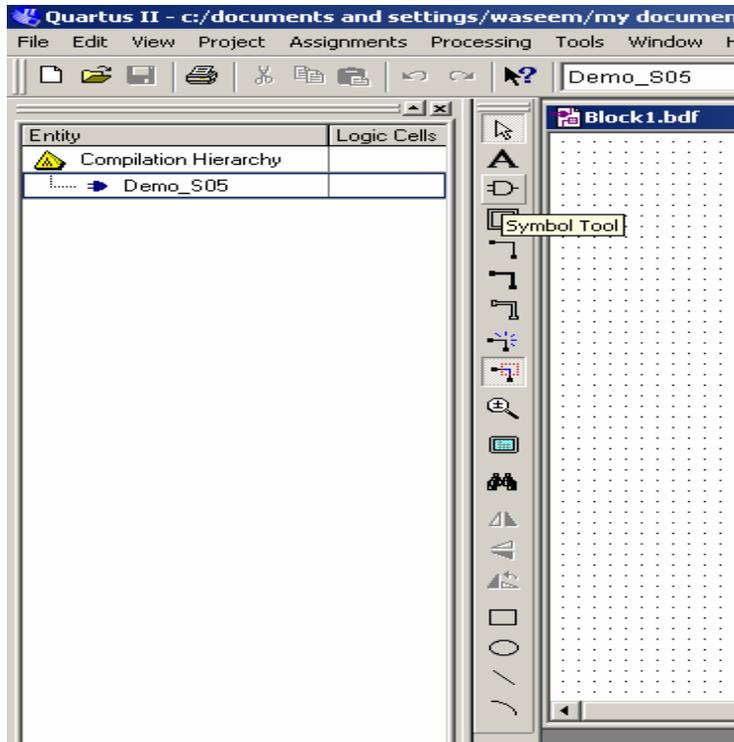


Figure8. Tools available with Schematic Editor where 'Symbol Tool' with the shape of an 'AND' gate is highlighted

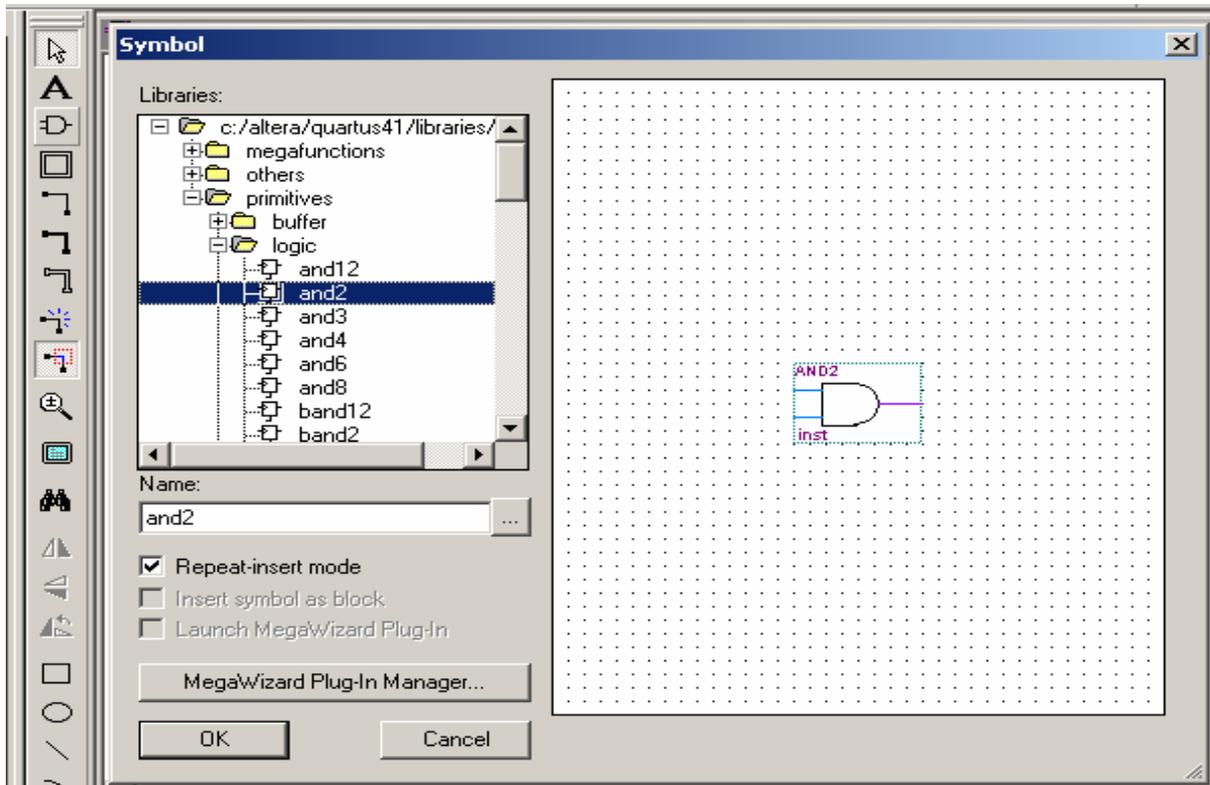


Figure9. Selecting a 2-input 'AND' gate using 'Symbol Tool'

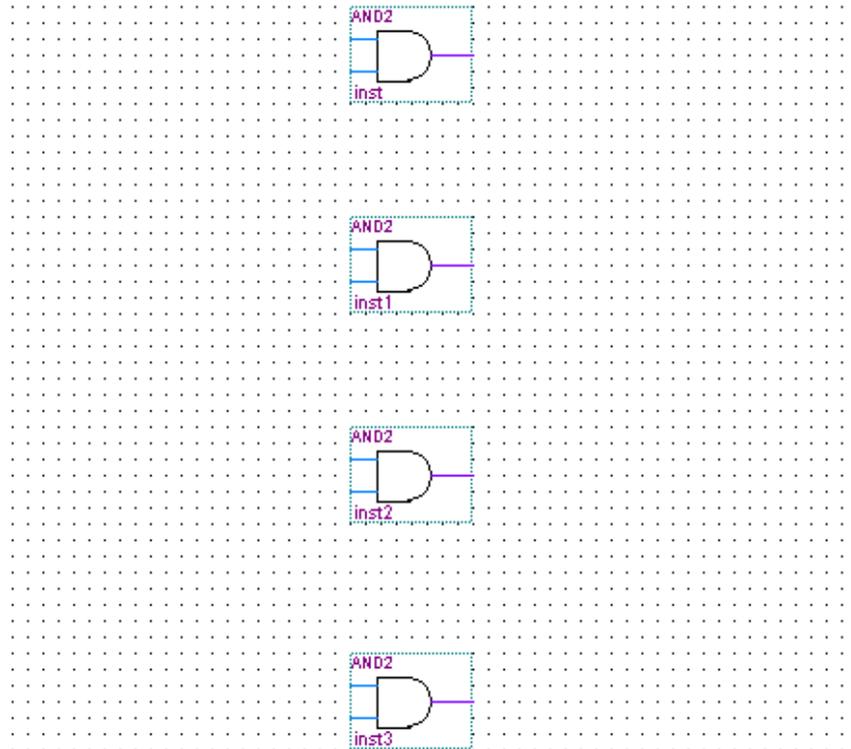


Figure10. Four AND gates placed on the schematic layout area.

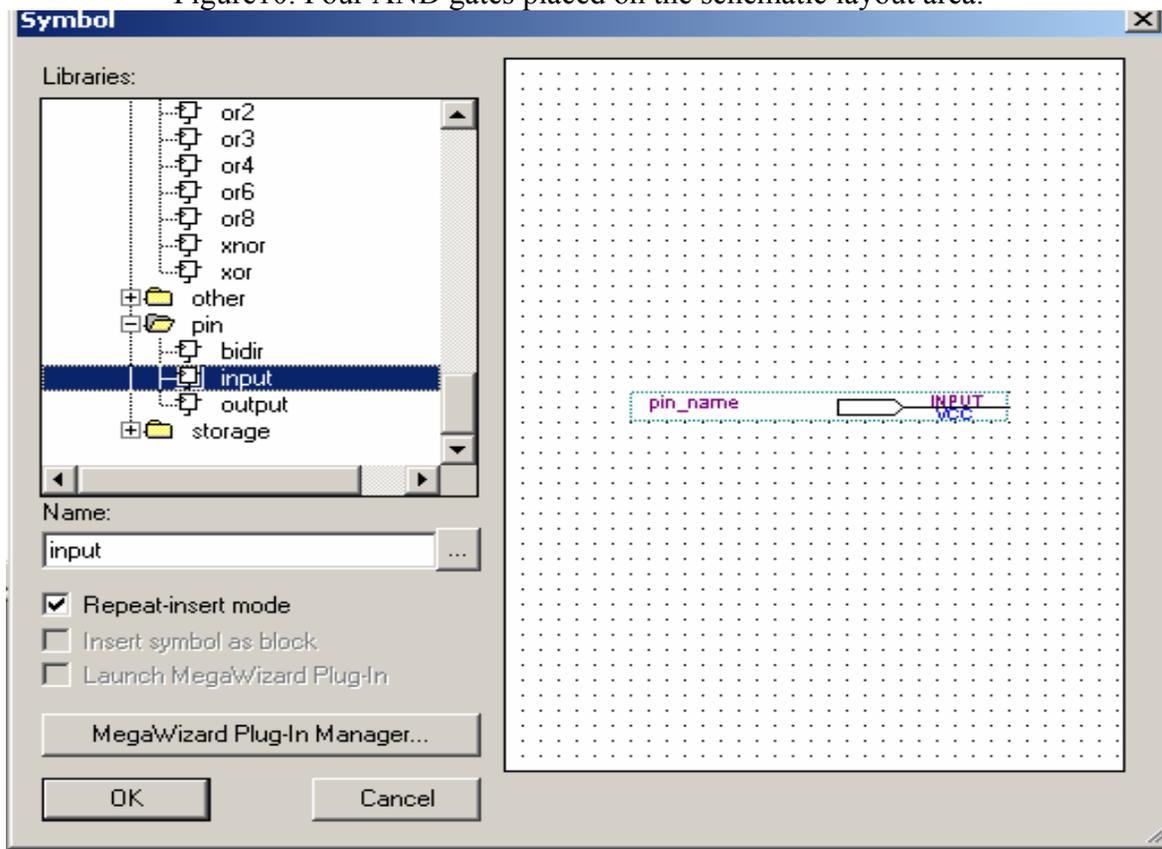


Figure11. Selecting an 'Input' pin using 'Symbol Tool'

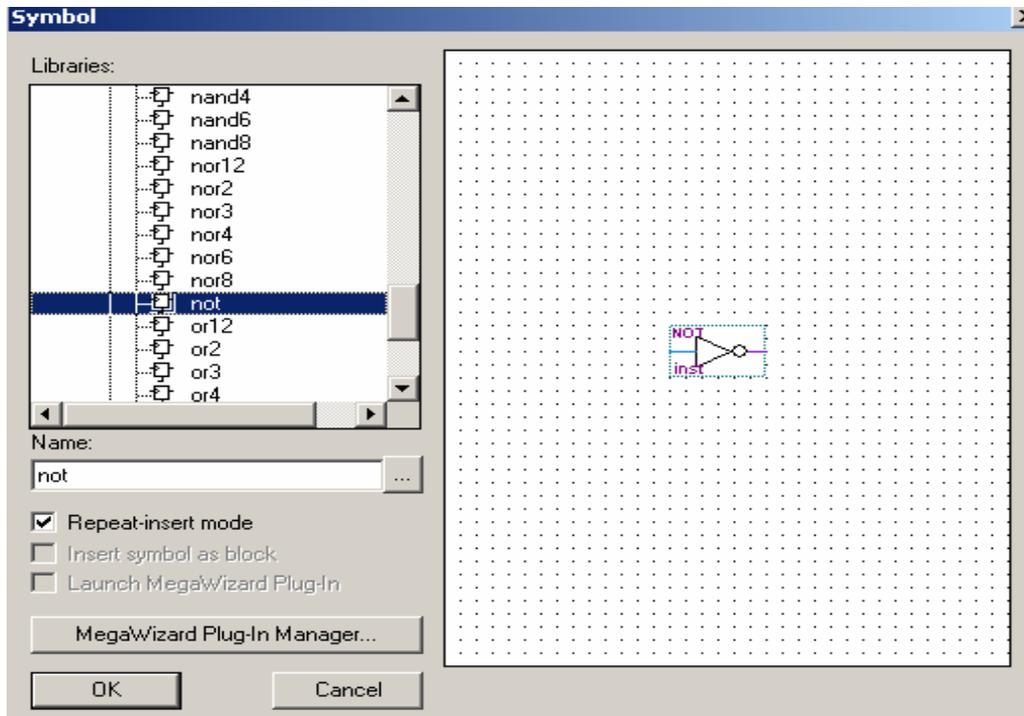


Figure12. Selecting a 'NOT' gate using 'Symbol Tool'

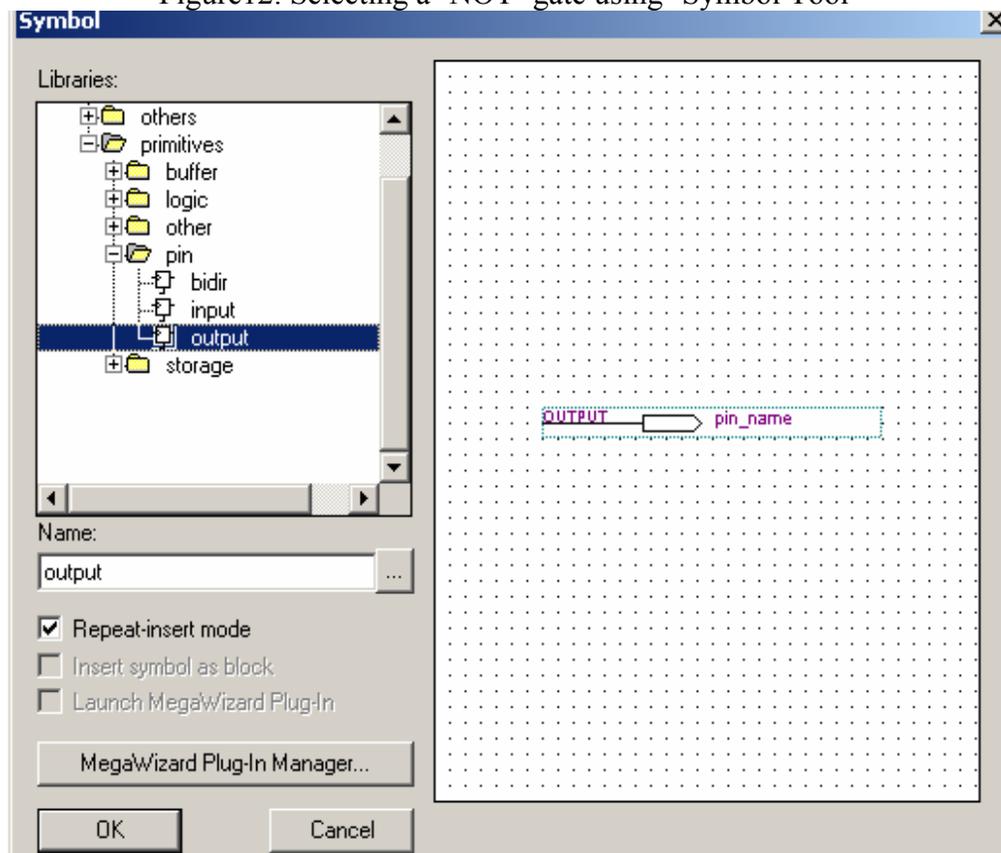


Figure13. Selecting an 'Output Pin' Using 'Symbol Tool'

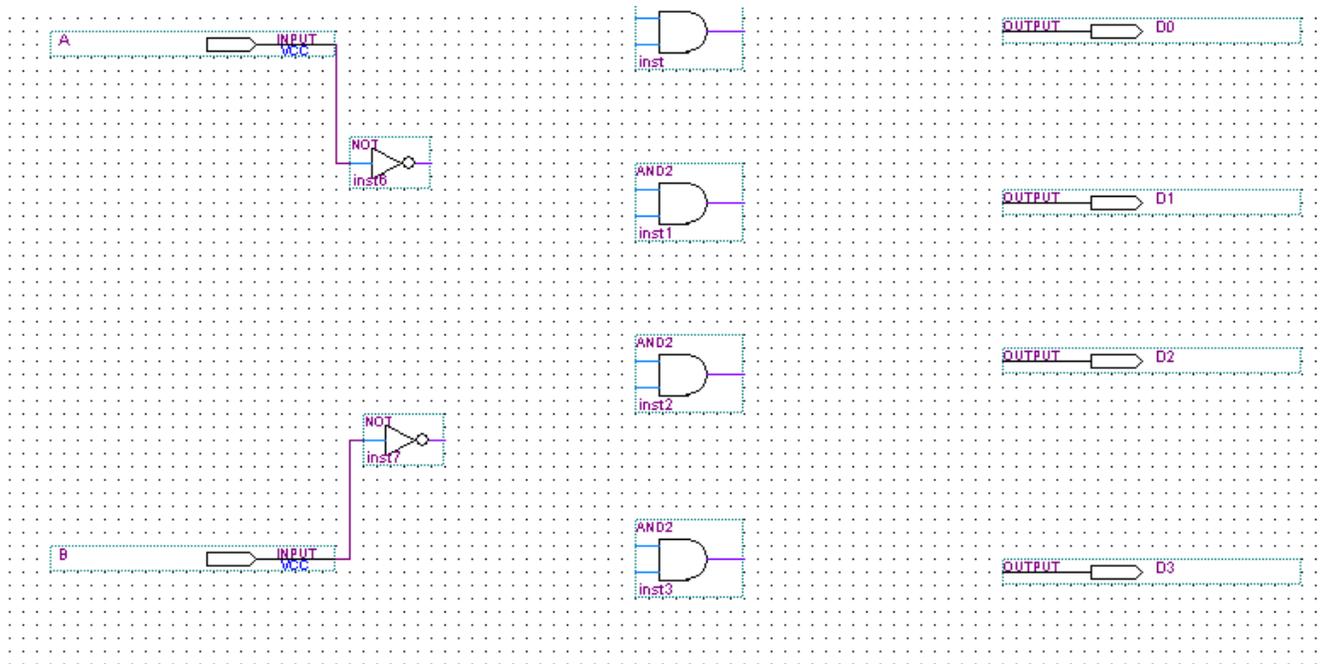


Figure14. All logic elements required for the 2 to 4 Decoder circuit, shown placed on Schematic design layout area

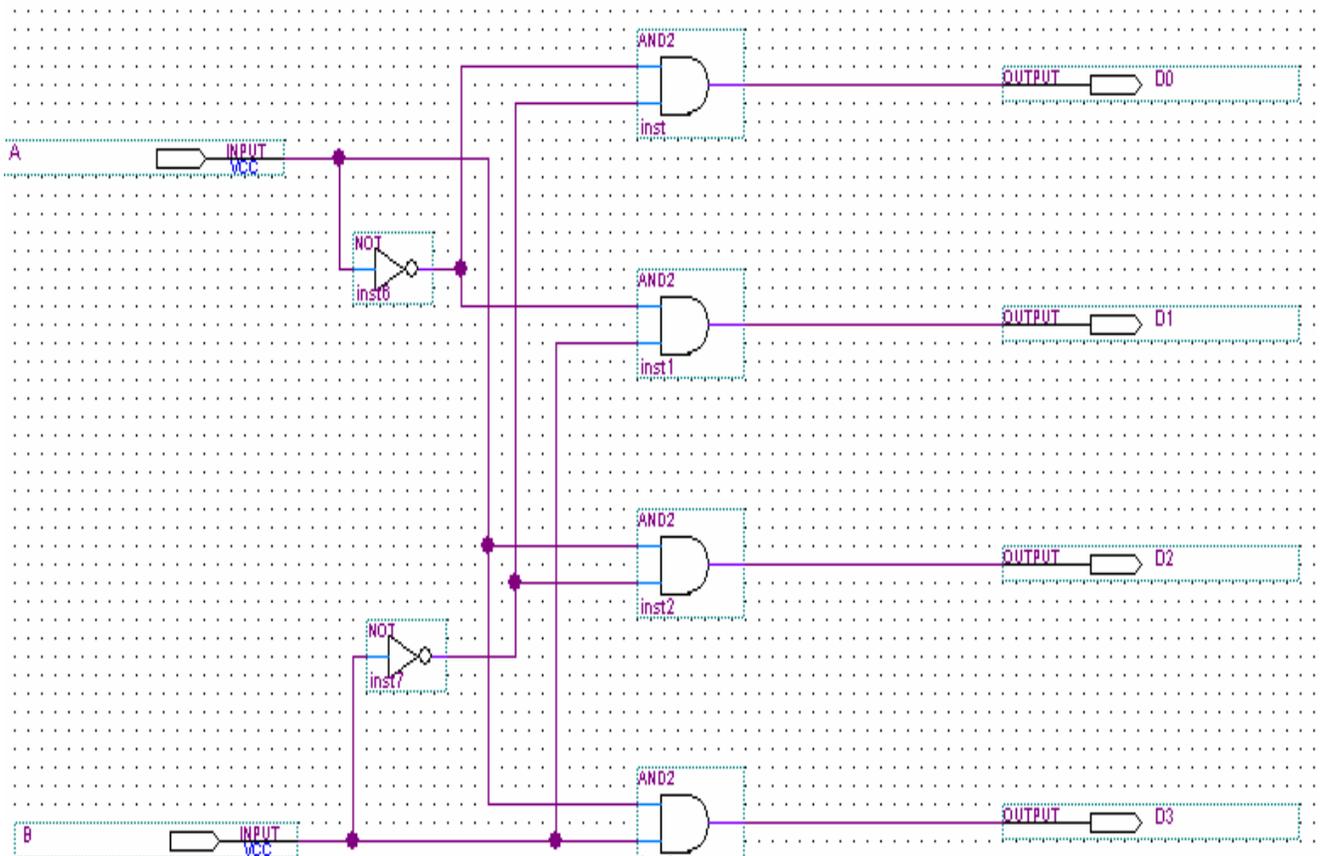


Figure15. Schematic design of the entire 2 to 4 Decoder circuit

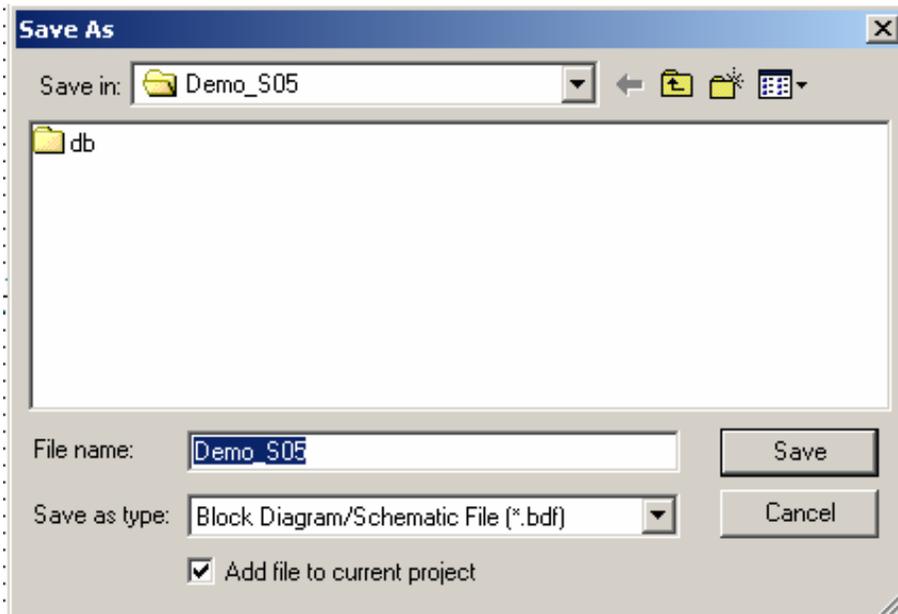


Figure16. Saving the schematic file, make sure that ‘Add File to current project’ checkbox is in checked state

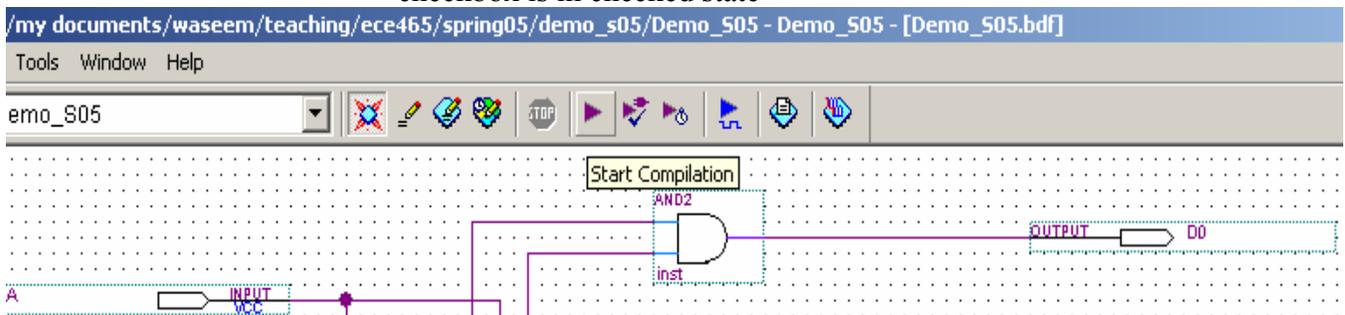


Figure17. Compiling the schematic design

3 Simulating Designed Circuits Using Quartus

In this section, we will follow the same step by step illustrative approach to go through each step required to perform simulation of the decoder circuit in the previous section.

First step is to create a new Simulation Input file. We will use the “Vector Waveform File” format to define simulation inputs. To create a new ‘Vector Waveform file’ we first go to file menu, select ‘New’ and then select ‘Vector Waveform File’ in the ‘Other Files’ tab on the ‘New File’ Dialog box. The step is shown in Figure18. After pressing OK on the “New File” Dialog box, we go to the ‘View’ menu, select ‘Utility Windows’ and then select ‘Node Finder’ as shown in Figure19. We will use ‘Node Finder’ to select input nodes of our newly designed circuit. What I have done here is to simply ask it to list all nodes by using the filter *pins: all* as illustrated in Figure20. Once it shows all the pins I select the input ones (represented by a preceding i on a pin shape) and drag them to the vector waveform file designated area for inputs as shown in Figure21.

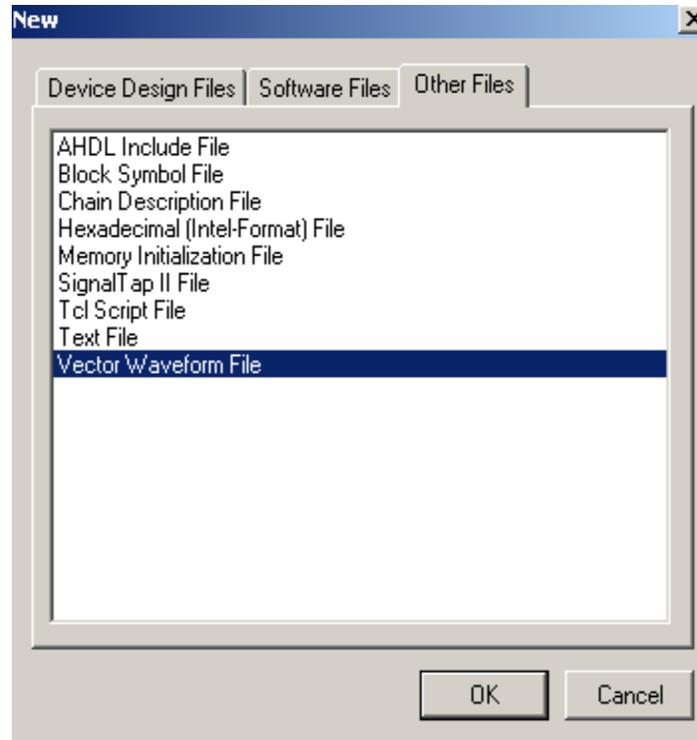


Figure18. 'New File' Dialog box for creating a new simulation file based upon 'Vector Waveform File' format

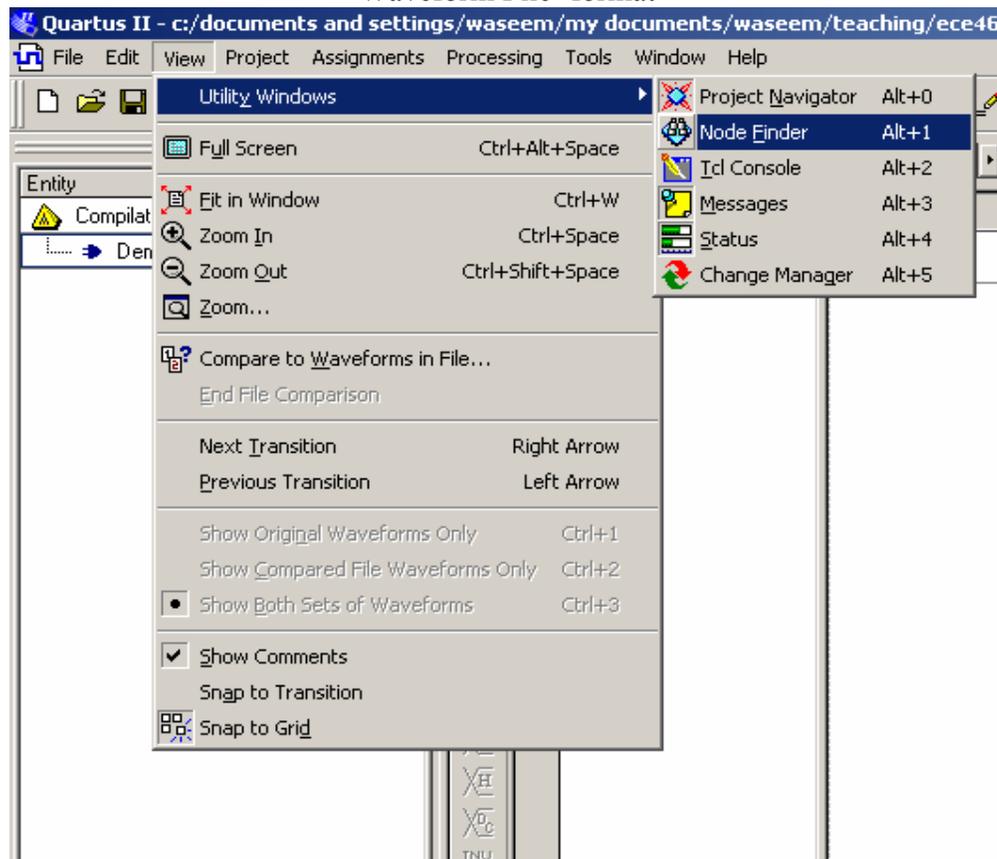


Figure19. Selecting the 'Node Finder' tool

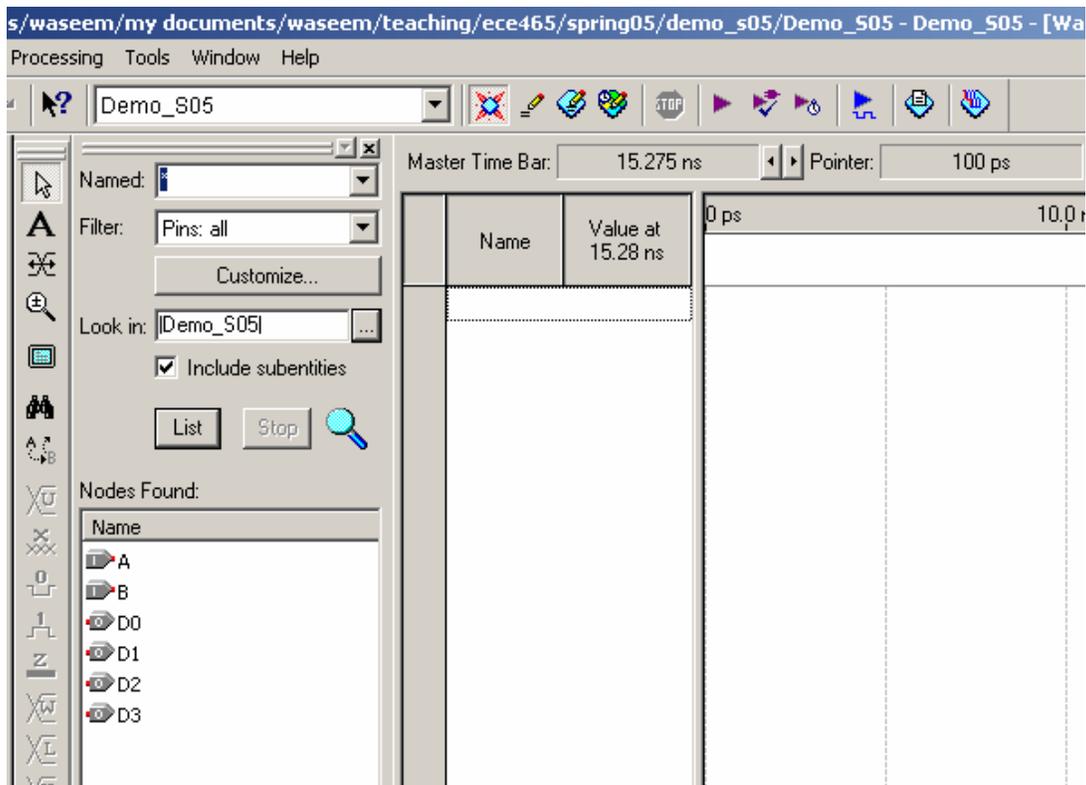


Figure20. The input and output nodes enumerated by 'Node Finder' tool

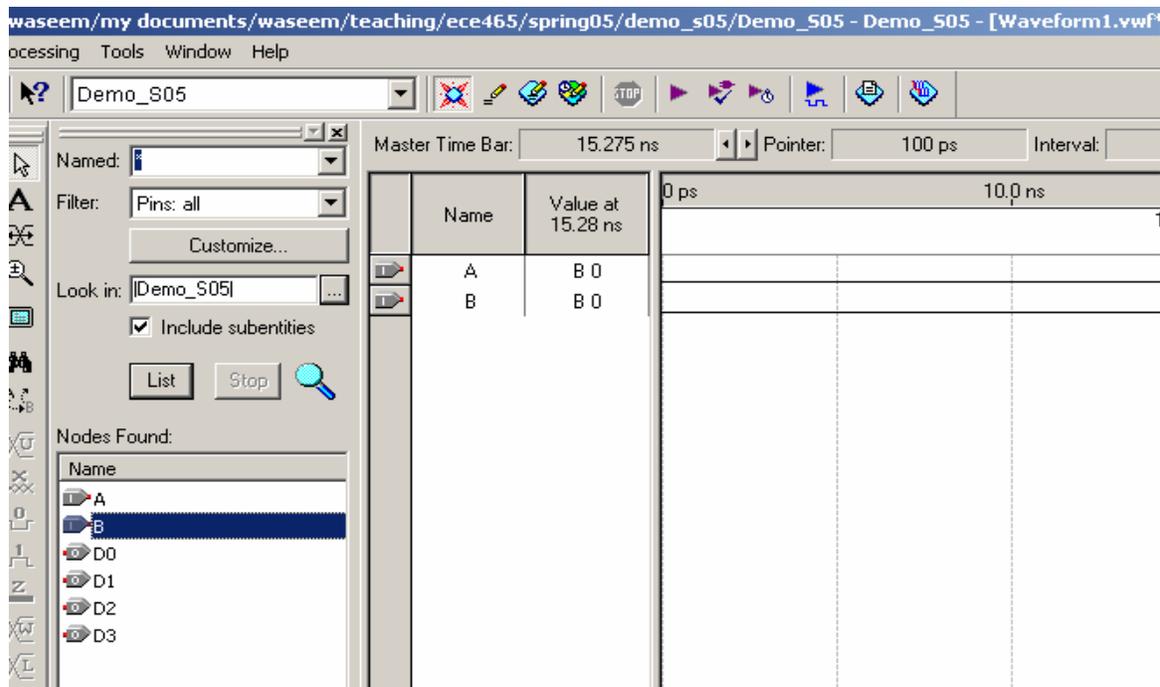


Figure21. Dragging input nodes onto the simulation input file.

Once we have dragged the input nodes on the Vector Waveform file, we will use the 'Waveform Editing Tool' (shown highlighted in Figure22) to create simulation waveforms for the inputs. For this, we simply select the 'Waveform Editing Tool' and drag it on the waveform area corresponding to the input for which we want to generate the waveform. Just by dragging mouse pointer, after selecting this tool, on the waveform area we can switch between logic low and logic high levels as shown in Figure23. Finally once we have generated the waveforms corresponding to all inputs (two in case of decoder) (Figure24) we save the simulation file (Figure25).



Figure22. The 'Waveform Editing Tool' highlighted

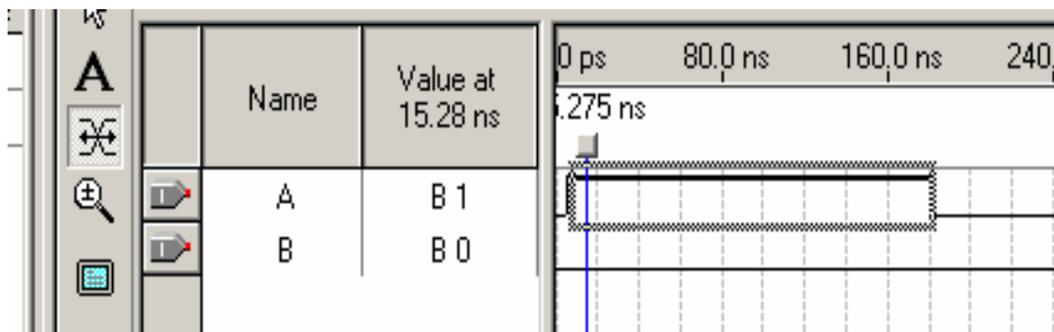


Figure23. Using 'Waveform Editing Tool' to create waveforms for input nodes A and B

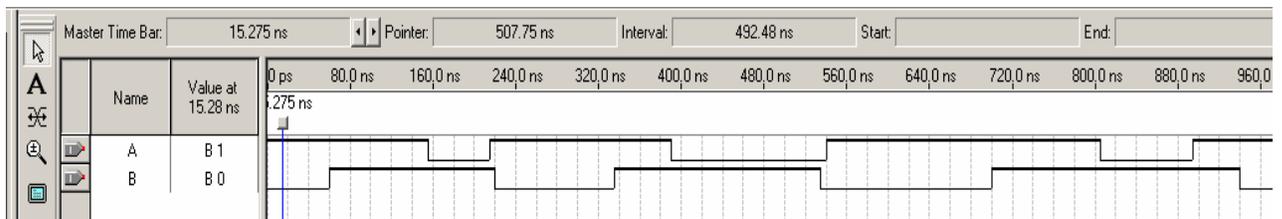


Figure24. The simulation waveforms for inputs A and B

After saving the simulation input 'Vector Waveform File'. We perform simulation by pressing 'Start Simulation' button (shown highlighted in Figure26). Once simulation is done successfully, we can see output waveforms corresponding to output pins on the Vector Waveform File as shown in Figure27.

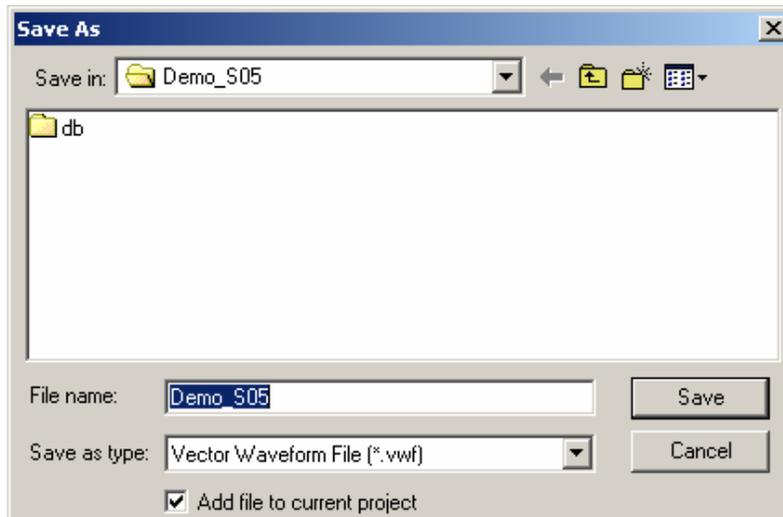


Figure25. Saving the 'Vector Waveform File' format based simulation input file for decoder circuit.



Figure26. "Start Simulation" button highlighted

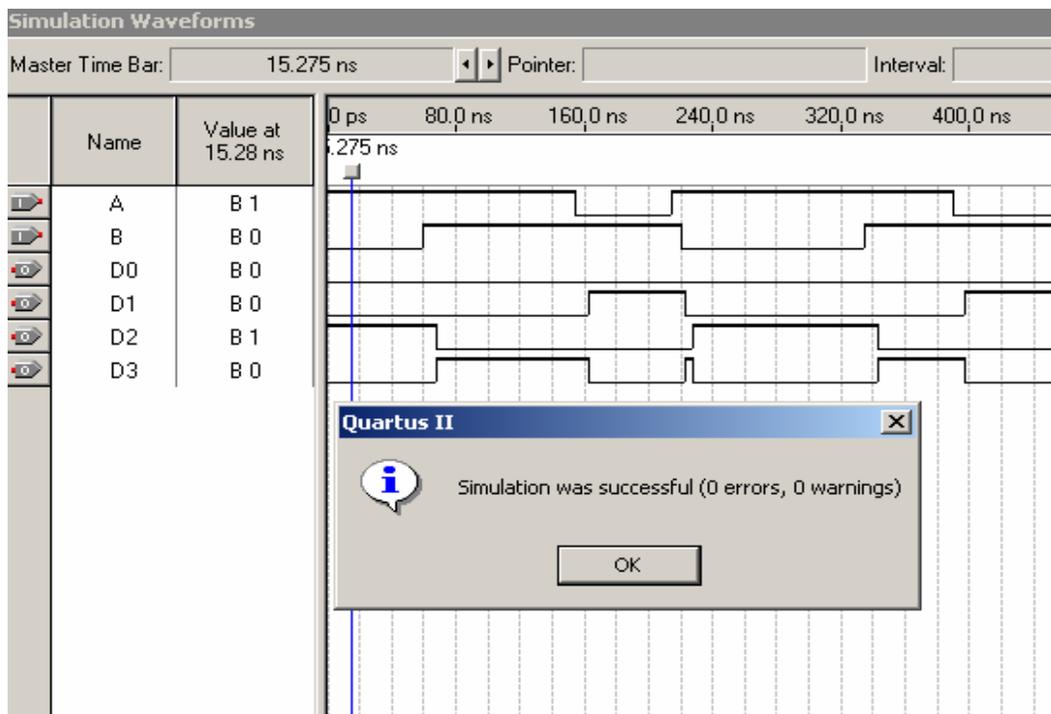


Figure27. Simulation Results

4 Conclusions

This tutorial is aimed at speeding up the time it takes for students to get themselves familiarized with Quartus II software. It gives an introduction to the software in a streamlined step by step approach. It does not, however, cover the details on Hardware Description Language (HDL) based design. Interested students are advised to explore the HDL based design functions provided by Quartus II, it will be extremely helpful for them in designing 'large' projects.

Finally, this document is a working draft, if you find any errors or inconsistencies or have any suggestions to add new sections, please direct them to wahmad@ece.uic.edu. I look forward to having your feedback.