Design of a UART

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Introduction

• A UART (Universal Asynchronous Receiver and Transmitter) is a device allowing the reception and transmission of information, in a serial and asynchronous way
• A UART allows the communication between a computer and several kinds of devices (printer, modem, etc), interconnected via an RS-232 cable
Serial transmission

• Data transmission is made by the UART in a serial way, by 11-bit blocks:
  • a 0 bit marks the starting point of the block
  • eight bits for data
  • one parity bit
  • a 1 bit marking the end of the block

• The transmission and reception lines should hold a 1 when no data is transmitted

- The first transmitted bit is the LSB (least significant bit)
- The parity bit is set to 1 or 0, depending on the number of 1's transmitted: if even parity is used, this number should be even; if odd parity is used, this number should be odd. If the chosen parity is not respected in the block, a transmission error should be detected
- The transmission speed is fixed, measured in bauds
• A possible entity for the UART is:

```
clk
reset
parityerr
framingerr
overrun
rxrdy
txrdy
read
write
datain
dataout
```

• The meaning of signals is:
  • **parityerr**: error during the block reception
  • **framingerr**: format error during the block reception
  • **overrun**: a new data is arrived before reading of the precedent data
  • **rxrdy**: a new data is arrived and it's ready for reading
  • **txrdy**: a new data is ready for sending
  • **read**: reading of the receiver's data is activated
  • **write**: writing of the emitter's data is activated
  • **data**: 8-bit data, read or written
  • **tx**: output bit
  • **rx**: input bit
• The UART can be divided into two modules: the receiver and the emitter

Data emission:
• to test if signal `txrdy` is active. If yes, a 8-bit data can be written in the emitter
• to place the 8-bit data in the input and to active the `write` signal
• the UART sends the 8 bits, via the `tx` signal. During transmission, the `txrdy` signal should be inactive
• at the end of the emission, `txrdy` should be active again et `tx` set to 1

Data reception:
• the 8 bits of information arrive in a serial way, at any moment, via the `rx` signal. The starting point is given par a 0 value of `rx`
• the UART places the 8 bits in a parallel way over `dataout`, and announces their availability setting `rxrdy` active
• the information reading is made active with the `read` signal
RS-232 connector

- The J3 connector provides a standard RS-232 connection
- The pins of J3 are directly connected to the FPGA, allowing an internal implementation of the serial controller
- It's possible to implement two UART without hardware handshaking

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- Or only one UART with hardware handshaking

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VHDL implementation